

REMARKS

The Final Office Action mailed March 26, 2002, has been received and reviewed. Claims 25, 26, 31 through 34, 37 through 40, and 43 through 49 are currently pending in the application. Claims 25, 26, 31 through 34, 37 through 40, and 43 through 49 stand rejected. Applicants propose to amend claims 25, 33, 39, and 46, and respectfully request reconsideration of the application as proposed to be amended herein.

Objection under 35 U.S.C. §132

The amendments filed on November 28, 2000 and on October 15, 2001 stand objected to under 35 U.S.C. §132 for allegedly introducing new matter into the disclosure. The examiner asserts that the limitation “a semiconductor substrate free of field oxide structures” is new matter. Applicants have amended claims 25, 33, 39, and 46 to recite “a semiconductor substrate having at least a portion free of field oxide structures.” Applicants respectfully traverse the new matter objection.

Applicants submit that the limitation “a semiconductor substrate having at least a portion free of field oxide structures” is supported by the drawings and by the specification of the as-filed application. Therefore, this limitation is not new matter because “information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter.” M.P.E.P. § 2163.06. In other words, amendments that are supported in the original description are not new matter. M.P.E.P. § 2163.07.

The examiner states that because the drawings are not drawn to scale, “the drawings by themselves can not be relied upon to claim the subject matters that are not disclosed.” Office Action of March 26, 2002, page 5 (emphasis in original). The examiner cites to M.P.E.P. § 2125 in support of this statement. However, M.P.E.P. § 2125 actually states that drawings may be used as prior art to anticipate claims if the drawings clearly show the structure that is claimed. M.P.E.P. § 2125 further states that the drawings may not be relied upon in support of arguments

based on the measurements of the drawing features unless the drawings are drawn to scale.

M.P.E.P. § 2125 (emphasis added). This is the only mention in M.P.E.P. § 2125 regarding the scale of the drawings. M.P.E.P. § 2125 does not state that subject matter depicted in drawings but not disclosed can not be claimed unless the drawings are drawn to scale. In contrast, M.P.E.P. § 2163.06 states that any “information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter.” Since the as-filed drawings of the present application show that at least a portion of the semiconductor substrate is free of field oxide structures, as discussed herein, this limitation is not new matter and may be added to the claims.

M.P.E.P. § 2125 also does not support the examiner’s assertion because applicants are not arguing about the measurements or scale of the field oxide structures. Rather, applicants submit that the as-filed drawings show that the field oxide structures do not exist before the annealing step but are present after the annealing step. Specifically, a comparison of FIGs. 1-3 and FIGs. 7-8 shows that the field oxide structures are absent in FIGs. 1-3 but are clearly present in FIGs. 7-8. Reference to the specification makes clear that FIGs. 1-3 depict the intermediate structure before the annealing step and FIGs. 7-8 show field oxide structures on the semiconductor substrate after the annealing step. As shown in FIGs. 1-3, the intermediate structure comprises, among other things, a semiconductor substrate having a first surface and a second surface, n-wells, p-wells, a pad oxide film, and a diffusion barrier layer. The semiconductor substrate does not comprise field oxide structures. In contrast, FIGs. 7-8 clearly show the presence of the field oxide structures, which are grown on the first surface of the semiconductor substrate after the high temperature anneal.

Since the drawings fully support the limitation of “a semiconductor substrate having at least a portion free of field oxide structures,” applicants submit that the new matter objections should be withdrawn. In addition to the drawings supporting this limitation, applicants submit that the specification fully supports this limitation. As discussed in applicants’ previous response, the specification discloses that the diffusion barrier is deposited on both surfaces of the

semiconductor substrate to encapsulate the substrate. The encapsulated substrate is then annealed to activate areas on the semiconductor substrate. After annealing, the field oxide structures are grown on the first surface of the substrate. Since the field oxide structures are only grown after annealing, the field oxide structures are not present on the semiconductor substrate before the intermediate structure is annealed. Therefore, since the field oxide structures are not present, the semiconductor substrate is necessarily "free of field oxide structures."

The examiner improperly uses the statement in the specification that the drawings "are not meant to be actual cross-sectional views of any particular portion of an actual semiconductor device, but are merely idealized representations which are employed to more clearly and fully depict the process of the invention than would otherwise be possible" in support of his assertion that the drawings are not drawn to scale and can not be relied upon to claim this subject matter. However, this statement in the specification does not mention the scale of the drawings. Rather, this statement states that the drawings show idealized semiconductor devices and are used to more clearly depict the invention.

Since the limitation "a semiconductor substrate having at least a portion free of field oxide structures" is supported by either or both of the drawings and/or the specification, applicants respectfully submit that the new matter objections be withdrawn.

35 U.S.C. § 112 Claim Rejections

Claims 25, 26, 31 through 34, 37 through 40, and 43 through 49 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

"An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, [and] diagrams . . . that fully set forth the claimed invention." M.P.E.P. § 2163. Furthermore,

“[p]ossession may be shown . . . by showing that the invention was ‘ready for patenting’ such as by the disclosure of drawings . . . that show that the invention was complete.” M.P.E.P. § 2163. As previously discussed, the drawings of the as-filed application clearly support that at least a portion of the semiconductor substrate is free of field oxide structures. Therefore, the as-filed drawings show that applicant was in possession of the claimed invention at the time the application was filed.

The examiner further contends that the drawings “at best” illustrate the absence of field oxide structures at the CMOS region. Office Action of March 26, 2002, page 6. To support this assertion, the examiner focuses on a statement in the background section of the application. However, as explicitly stated later in the application, the claimed invention “can be used to form any MOS structure such as NMOS structures or PMOS structures, or any semiconductor structure using a LOCOS-type field isolation structure.” Page 10, lines 22-25.

“[N]ewly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure” but there is no *in haec verba* requirement. M.P.E.P. § 2163. The examiner states that the as-filed specification does not explicitly or implicitly support the contention that at least a portion of the semiconductor substrate is free of field oxide structures. Office Action of March 26, 2002, page 6. However, applicants submit that the as-filed drawings disclose that at least a portion of the semiconductor substrate is free of field oxide structures, for the reasons discussed above for the 35 U.S.C. § 132 objections.

In addition, the as-filed specification discloses that at least a portion of the semiconductor substrate is free of field oxide structures, as discussed above with the 35 U.S.C. § 132 objections. In further support of the disclosure of this limitation, the as-filed specification states that the “densification of the substrate resulting from the annealing prior to the formation of the isolation structure reduces the encroachment of the isolation structure. Page 10, lines 5-7 (emphasis added). Since the specification explicitly states that the field oxide structures are formed after annealing, this further implies that the field oxide structures are not present before annealing.

Since the as-filed drawings and specification disclose that at least a portion of the semiconductor substrate is free of field oxide structures, applicants request that the 35 U.S.C. § 112 rejections of claims 25, 26, 31 through 34, 37 through 40, and 43 through 49 be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Claims 25, 26, 31, 33, 34, 37 through 40, and 43 through 48 stand rejected under 35 U.S.C. § 103(a) ("Section 103") as being unpatentable over U.S. Patent No. 5,545,577 issued to Tada ("Tada") in view of U.S. Patent No. 5,874,325 issued to Koike ("Koike"). Claims 32 and 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tada and Koike and further in view of U.S. Patent No. 5,846,596 issued to Shim *et al.* ("Shim"). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The examiner bears the burden of establishing that each of these three criteria is met. If one of these criteria is not met, the examiner has not established a *prima facie* case of obviousness.

Obviousness Rejection Based On Tada In View Of Koike

Claims 25, 26, 31, 33, 34, 37 through 40, and 43 through 48 stand rejected under Section 103 as being unpatentable over Tada in view of Koike. Applicants respectfully submit that a *prima facie* case of obviousness has not been established because Tada and Koike do not teach or

suggest all the limitations of the claimed invention and do not provide a motivation to combine to produce the claimed invention.

As amended, independent claim 25 recites an intermediate structure in the formation of an isolation structure that, among other things, includes a semiconductor substrate having at least a portion that is free of field oxide structures. The semiconductor substrate also has a first and a second opposing surface. The semiconductor substrate has p-wells and n-wells on its first surface. The p-wells comprise at least one activated, annealed n-type area and the n-wells comprise at least one activated, annealed p-type area. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion layer that extends over both the first and second surfaces of the substrate, thereby encapsulating the semiconductor substrate.

In contrast, Tada discloses a method of producing a semiconductor device that has two MIS transistor circuits on a first surface of the device. A silicon nitride layer is used as a mask to form a field oxide film on the first surface of the semiconductor substrate. As a result, gate oxides of different thicknesses are produced without contact the resist layer, thus reducing contamination due to the resist.

Koike discloses a method of manufacturing a semiconductor device that includes a gettering layer. The gettering layer is comprised of a silicon thin film to which impurities have been added. The silicon thin film is applied to both surfaces of a semiconductor surface. Silicon nitride layers are then deposited over the silicon thin film to protect the gettering properties of the silicon thin film layers until the manufacturing process is complete.

As acknowledged by the examiner, Tada does not teach or suggest the limitation of a substantially dopant-free, uninterrupted barrier layer that extends over the second surface of the substrate. Office Action of March 26, 2002, page 3. In addition, Tada necessarily does not disclose that the intermediate structure is encapsulated because Tada does not disclose that the barrier layer extends over the second surface of the substrate. Furthermore, Tada does not teach or suggest that the p-wells and n-wells comprise activated, annealed n-type and p-type areas, respectively.

While Koike discloses that its silicon nitride layer extends over both the first and second surfaces of the substrate, Koike does not disclose p-wells and n-wells on the first surface of the substrate or activated, annealed n-type and p-type areas within the p-well and n-wells, respectively.

In addition, the examiner has not provided a convincing motivation to combine the cited references to produce the claimed invention. The examiner states that it would have been obvious to one of ordinary skill in the art to encapsulate the semiconductor substrate of Tada to prevent the second surface from oxidizing. Office Action of March 26, 2002, page 3. The examiner also asserts that applicants have agreed to this motivation to combine. Office Action of March 26, 2002, page 8.

However, applicants have not agreed to a motivation to combine the cited references. The examiner has not identified a location in the record to support this [?]assertion. Furthermore, review of the record indicates that applicants have argued against any motivation to combine the cited references. See for example applicants' response filed on October 15, 2001; applicants' supplemental response to final rejection filed on July 5, 2001; applicants' response filed on April 12, 2001; applicants' response filed on November 28, 2000; applicants' response filed on July 14, 2002; applicants' response filed on June 19, 2000; and applicants' response filed on February 3, 2000.

As explained most recently in applicants' response filed on October 15, 2001, the cited references do not provide a motivation to combine because "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." M.P.E.P. § 2143.01. Moreover, the fact that the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without an objective reason to combine the teachings of the references. *Id.* Neither Tada nor Koike provide any motivation or suggestion to combine their teachings to produce the invention of claim 25. Tada does not suggest the desirability of its second surface having a substantially dopant-free, uninterrupted

barrier layer. In addition, while Koike discloses using the silicon nitride layer on both surfaces to protect the gettering properties of the underlying layers, Koike does not suggest the desirability of forming silicon nitride layers on both surfaces of other semiconductor substrates, such as the substrate disclosed in Tada. Furthermore, the examiner has not provided an objective reason to combine Tada and Koike. While the examiner asserts that the motivation is to prevent oxidation of the second surface of the substrate, the claimed invention discloses that the substantially dopant-free, uninterrupted-diffusion barrier layer is applied to reduce encroachment of isolation structures, not to prevent oxidation. Therefore, one of ordinary skill in the art would not be motivated to produce the invention of claim 25 after reading Tada and Koike.

Since Tada and Koike do not teach or suggest all the limitations of claim 25 and do not provide a motivation to combine, applicants respectfully submit that a *prima facie* case of obviousness of claim 25 has not been established. Therefore, applicants respectfully request that the rejection of claim 25 be withdrawn.

Dependent claims 26 and 31 include all of the claim limitations of claim 25 and, therefore, are allowable, *inter alia*, as depending from an allowable claim.

Claim 33 stands rejected under Section 103 as being unpatentable over Tada in view of Koike. Applicants respectfully submit that the rejection of claim 33 is improper because Tada and Koike do not teach or suggest all of the claim limitations and do not provide a suggestion or motivation to combine to produce the claimed invention.

As amended, claim 33 recites an intermediate structure in the formation of an isolation structure for a semiconductor device. The intermediate structure comprises a semiconductor substrate having at least a portion that is free of field oxide structures. The semiconductor substrate also has a first and second surface. The semiconductor substrate has at least one p-well and at least one n-well on its first surface. The p-wells and n-wells comprise at least one activated, annealed dope area. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion barrier layer that extends over both the first and second surfaces of the substrate, thereby encapsulating the semiconductor substrate.

Applicants submit that Tada and Koike do not teach or suggest all of the limitations of claim 33 and do not provide a motivation to combine to produce the claimed invention for the same reasons discussed above for claim 25. Therefore, applicants submit that a *prima facie* case of obviousness of claim 33 has not been established and request that the rejection of claim 33 be withdrawn.

Dependent claims 34, 37, and 38 include all of the claim limitations of claim 33 and, therefore, are allowable, *inter alia*, as depending from an allowable claim.

Claim 39 stands rejected under Section 103 as being unpatentable over Tada in view of Koike. Applicants respectfully submit that the rejection of claim 39 is improper because Tada and Koike do not teach or suggest all of the claim limitations and do not provide any suggestion or motivation to combine the references.

As amended, claim 39 recites an intermediate structure in the formation of an isolation structure for a semiconductor device. The intermediate structure comprises a semiconductor substrate that has at least a portion free of field oxide structures. The semiconductor substrate also has a first surface and a second surface. The semiconductor substrate has at least one activated, annealed first doped area on its first surface and at least one activated, annealed second, differently doped area within the at least one first doped area. The intermediate structure also comprises a substantially dopant-free, uninterrupted diffusion barrier layer that extends over the first and second surfaces of the semiconductor substrate, thereby encapsulating the semiconductor substrate.

Tada and Koike do not teach or suggest the limitations of claim 39 and do not provide a motivation to combine to produce the claimed invention for the same reasons discussed above with claim 25. Therefore, applicants submit that a *prima facie* case of obviousness of claim 39 has not been established and request that the rejection of claim 39 be withdrawn.

Dependent claims 40 and 43-45 include all of the claim limitations of claim 39 and, therefore, are allowable, *inter alia*, as depending from an allowable claim.

Claim 46 stands rejected under Section 103 as being unpatentable over Tada in view of Koike. Applicants respectfully submit that the rejection of claim 46 is improper because Tada and Koike do not teach or suggest all of the claim limitations and do not provide a suggestion or motivation to combine the references to produce the claimed invention.

As amended, claim 46 recites an intermediate structure useful in the formation of electrical device isolation structures. The intermediate structure comprises a semiconductor substrate that has at least a portion that is free of field oxide structures. The semiconductor substrate also includes a first surface and a second surface, with the first surface opposing the second surface. The semiconductor also has at least one p-well and at least one n-well defined on its first surface. In addition, at least one activated, annealed p-type area is defined within the one n-well and at least one activated, annealed n-type area is defined within the p-well. A substantially dopant-free, uninterrupted diffusion barrier layer extends over the first and second surfaces, thereby encapsulating the semiconductor substrate.

Tada and Koike do not teach or suggest the limitations of claim 46 and do not provide a motivation to combine to produce the claimed invention, for the same reasons discussed above with claim 25. Therefore, applicants submit that a *prima facie* case of obviousness of claim 46 has not been established and respectfully request that the rejection of claim 46 be withdrawn.

Dependent claims 47 and 48 include all of the claim limitations of claim 46 and, therefore, are allowable, *inter alia*, as depending from an allowable claim.

Obviousness Rejection Based on Tada and Koike and Further in View of Shim

Claims 32 and 49 stand rejected under Section 103 as being unpatentable over Tada and Koike, as applied to claims 25 and 46 above, and further in view of Shim. Applicants respectfully traverse this rejection, as hereinafter set forth.

Since claim 32 depends from claim 25, it includes all the claim limitations of claim 25. Therefore, as amended, claim 32 recites an intermediate structure in the formation of an isolation structure that, among other things, includes a semiconductor substrate having at least a portion

that is free of field oxide structures. The semiconductor substrate also has a first and a second opposing surface. The semiconductor substrate has p-wells and n-wells on its first surface. The p-wells comprise at least one activated, annealed n-type area and the n-wells comprise at least one activated, annealed p-type area. The intermediate structure also has a substantially dopant-free, uninterrupted diffusion layer that extends over both the first and second surfaces of the substrate, thereby encapsulating the semiconductor substrate. The substantially dopant-free, uninterrupted diffusion barrier layer is silicon oxynitride.

Claim 32 is not obvious for the reasons discussed above for claim 25 because Shim does not cure the deficiencies in Tada and Koike. Specifically, Shim does not provide a motivation to combine the references and does not teach or suggest the claim limitations that are not taught or suggested by Tada and Koike. Finally, the nonobviousness of independent claim 25 precludes the rejection of claim 32, which depends from claim 25, because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); *see also* M.P.E.P. § 2143.03.

Since a *prima facie* case of obviousness has not been established, applicants respectfully request that the rejection of claim 32 be withdrawn.

Similarly, since claim 49 depends from claim 46, it includes all the claim limitations of claim 46. Therefore, as amended, claim 49 recites an intermediate structure useful in the formation of electrical device isolation structures. The intermediate structure comprises a semiconductor substrate that has at least a portion that is free of field oxide structures. The semiconductor substrate also includes a first surface and a second surface, with the first surface opposing the second surface. The semiconductor also has at least one p-well and at least one n-well defined on its first surface. In addition, at least one activated, annealed p-type area is defined within the one n-well and at least one activated, annealed n-type area is defined within the p-well. A substantially dopant-free, uninterrupted diffusion barrier layer extends over the first and second surfaces, thereby encapsulating the semiconductor substrate. The substantially dopant-free, uninterrupted diffusion barrier layer recited in claim 49 is silicon oxynitride

5

Claim 49 is not obvious for the same reasons discussed above for claim 46 because Shim does not cure the deficiencies in Tada and Koike. Shim does not teach or suggest all of the claim limitations and does not provide a motivation to combine the references. Finally, the nonobviousness of independent claim 46 precludes the rejection of claim 46, which depends from claim 49, because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); *see also* M.P.E.P. § 2143.03.

Since a *prima facie* case of obviousness has not been established, applicants respectfully submit that the rejection of claim 49 be withdrawn.

ENTRY OF AMENDMENTS

The proposed amendments to claims 25, 33, 39, and 46 above should be entered by the examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 25, 26, 31 through 34, 37 through 40, and 43 through 49 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact applicants' undersigned attorney.

Respectfully Submitted,

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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

25. (Seven times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:
a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;
at least one p-well and at least one n-well on said substrate first surface;
at least one activated, annealed p-type area within said at least one n-well and at least one activated, annealed n-type area within said at least one p-well; and
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

33. (Five times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:
a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;
at least one p-well and at least one n-well on said substrate first surface;
at least one activated, annealed doped area within at least one of said at least one n-well and said at least one p-well; and
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

39. (Five times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:
a semiconductor substrate having at least a portion free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;
at least one activated, annealed first doped area on said substrate first surface;
at least one activated, annealed second, differently doped area within said at least one first doped area; and
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

46. (Three times amended) An intermediate structure useful in the formation of electrical device isolation structures, comprising:
a semiconductor substrate having at least a portion that is free of field oxide structures and includes a first surface and a second surface, said first surface opposing said second surface;
at least one p-well and at least one n-well defined on said first surface of said substrate;
at least one activated, annealed p-type area defined within said at least one n-well and at least one activated, annealed n-type area defined within said at least one p-well; and
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.